DATA SHEET

BLV57
UHF linear push-pull power transistor

Product specification
Supersedes data of August 1986

1998 Feb 09

Philips Semiconductors

PHILIPS

UHF linear push-pull power transistor BLV57

FEATURES

- internally matched input for wideband operation and high power gain
- internal midpoint (r.f. ground) reduces negative feedback and improves power gain
- increased input and output impedances (compared with single-ended transistors) simplify wideband matching
- length of the external emitter leads is not critical
- diffused emitter ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability.

DESCRIPTION

Two n-p-n silicon planar epitaxial transistor sections in one package to be used as push-pull amplifier, primarily intended for use in linear u.h.f. television transmitters and transposers.

The package is an 8-lead flange type with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT161A

PIN	SYMBOL	DESCRIPTION
1	e	emitter
2	e	emitter
3	c2	collector 2
4	b2	base 2
5	c1	collector 1
6	b1	base 1
7	e	emitter
8	e	emitter

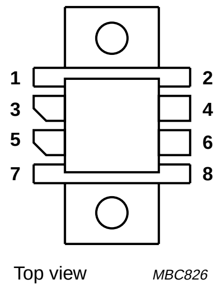

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

R.F. performance in linear amplifier

MODE OF OPERATION	f_{vision} MHz	V_{CE} V	$I_{C1} = I_{C2}$ A	$I_{C(ZS)}$ A	T_h °C	d_{im}(1) dB	$P_{o\ sync}$(1) W	P_L W	G_p dB
class-A	860	25	0,85	–	70	–60	〉 6	–	〉 8,0
					25	–55	typ. 12		typ. 9,0
class-AB	860	25	1,25	2 × 0,1	25	–	–	typ. 38(2)	typ. 6,5(2)

Notes

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak sync level.
2. Power gain compression is 1 dB.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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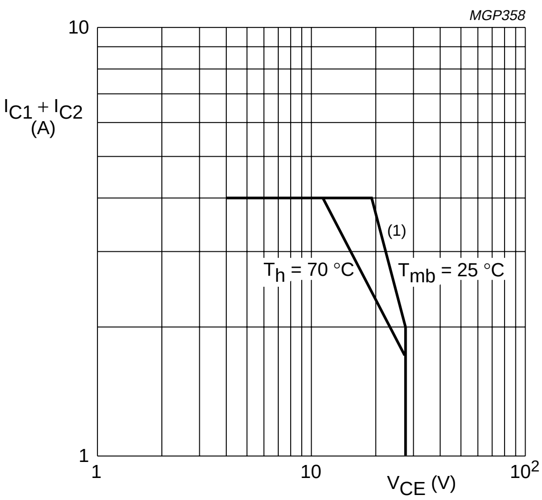
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage				
(peak value); $V_{BE} = 0$	v_{CESM}	max.	50	V
open base	V_{CEO}	max.	27	V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5	V
Collector current per transistor section				
d.c. or average	I_C; $I_{C(AV)}$	max.	2	A
(peak value); f 〉 1 MHz	I_{CM}	max.	4	A
Total power dissipation at T_{mb} = 25 °C[(1)]	P_{tot}	max.	77	W[(1)]
R.F. power dissipation (f 〉 1 MHz); T_{mb} = 25 °C[(1)]	P_{rf}	max.	93	W[(1)]
Storage temperature	T_{stg}	–65 to + 150		°C
Operating junction temperature	T_j	max.	200	°C

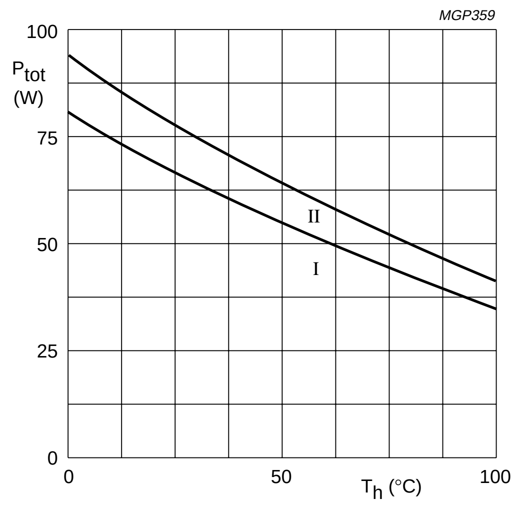
Note

1. Dissipation of either transistor section should not exceed half rated dissipation.



(1) Second breakdown limit (independent of temperature).

Fig.2 D.C. SOAR.[(1)]



I Continuous d.c. (including r.f. class-A) operation
II Continuous r.f. operation
Dissipation of either transistor section should not exceed half rated dissipation.

Fig.3 Power derating curves vs. temperature.(1)

THERMAL RESISTANCE

(dissipation = 42 W; T_{mb} = 80,5 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j-mb(dc)}$	=	2,43	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j-mb(rf)}$	=	1,91	K/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0,25	K/W

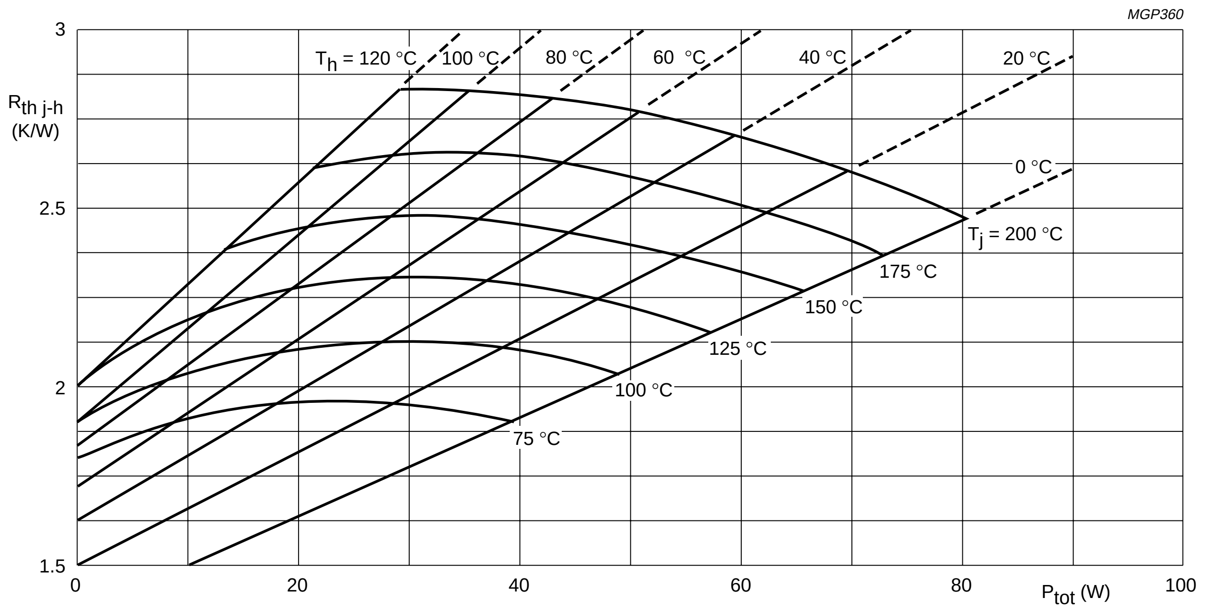


Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb\text{-}h}$ = 0,25 K/W.)

Example

Nominal class-A push-pull operation (without r.f. signal): V_{CE} = 25 V; I_{C1} = I_{C2} = 0,85 A; T_h = 70 °C.

Fig.4 shows:	$R_{th\ j\text{-}h}$	max.	2,68	K/W
	T_j	max.	184	°C
Typical device:	$R_{th\ j\text{-}h}$	typ.	2,28	K/W
	T_j	typ.	167	°C

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CHARACTERISTICS apply to either transistor section unless otherwise specified

T_j = 25°C

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 10 mA	$V_{(BR)CES}$	⟩	50	V
open base; I_C = 25 mA	$V_{(BR)CEO}$	⟩	27	V
Emitter-base breakdown voltage				
open collector; I_E = 5 mA	$V_{(BR)EBO}$	⟩	3,5	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 27 V	I_{CES}	⟨	10	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	⟩	2	mJ
R_{BE} = 10 Ω	E_{SBR}	⟩	2	mJ
D.C. current gain(1)				
I_C = 0,85 A; V_{CE} = 25 V	h_{FE}	⟩ typ.	15 40	
D.C. current gain ratio of transistor sections				
I_C = 0,85 A; V_{CE} = 25 V			0,67 to 1,5	
Collector-emitter saturation voltage(1)				
I_C = 1,7 A; I_B = 0,17 A	V_{CEsat}	typ.	0,75	V
Transition frequency at f = 100 MHz(2)				
$-I_E$ = 0,85 A; V_{CB} = 25 V	f_T	typ.	2,5	GHz
$-I_E$ = 1,7 A; V_{CB} = 25 V	f_T	typ.	2,5	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 25 V	C_c	typ. ⟨	24 30	pF pF
Feedback capacitance at f = 1 MHz				
I_C = 50 mA; V_{CE} = 25 V	C_{re}	typ.	15	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0,02$.
2. Measured under pulse conditions: $t_p \leq 50$ µs; $\delta \leq 0,01$.

The graphs apply to either transistor section.

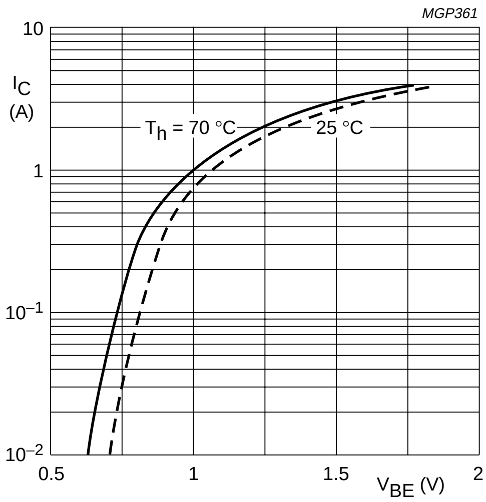


Fig.5 Typical values; V_{CE} = 25 V.

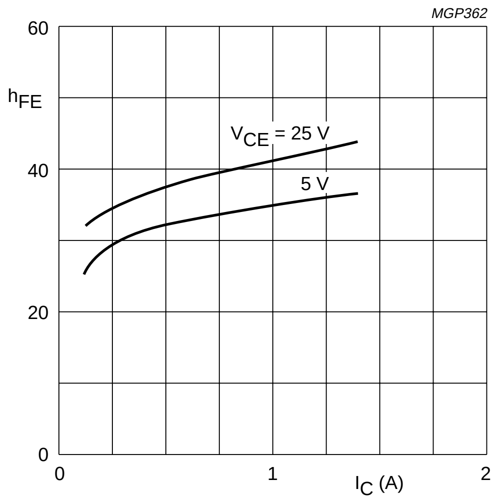


Fig.6 Typical values; T_j = 25 °C.

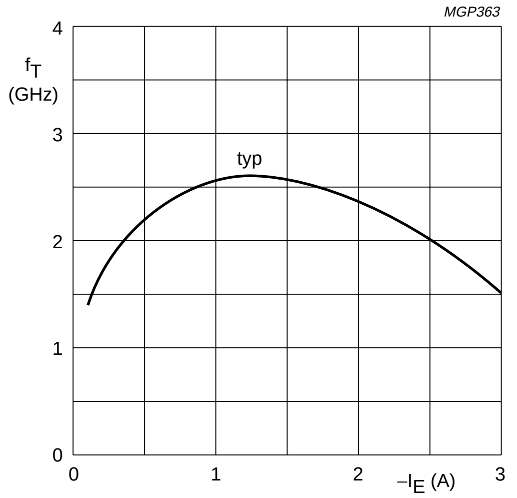


Fig.7 V_{CB} = 25 V; f = 500 MHz; T_j = 25 °C.

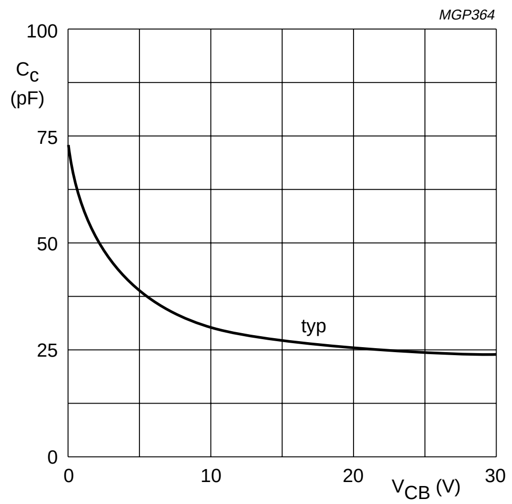


Fig.8 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in u.h.f. class-A operation (linear push-pull power amplifier)

f_{vision} (MHz)	V_{CE} (V)	$I_{C1} = I_{C2}$ (A)	T_h (°C)	d_{im} [1] (dB)	$P_{o\ sync}$ [1] (W)	G_p (dB)
860	25	0,85	70	–60	〉 6	〉 8,0
			70	–60	typ. 7,5	typ. 8,5
			70	–55	typ. 10	typ. 8,5
			25	–55	typ. 12	typ. 9,0

Note

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak sync level.

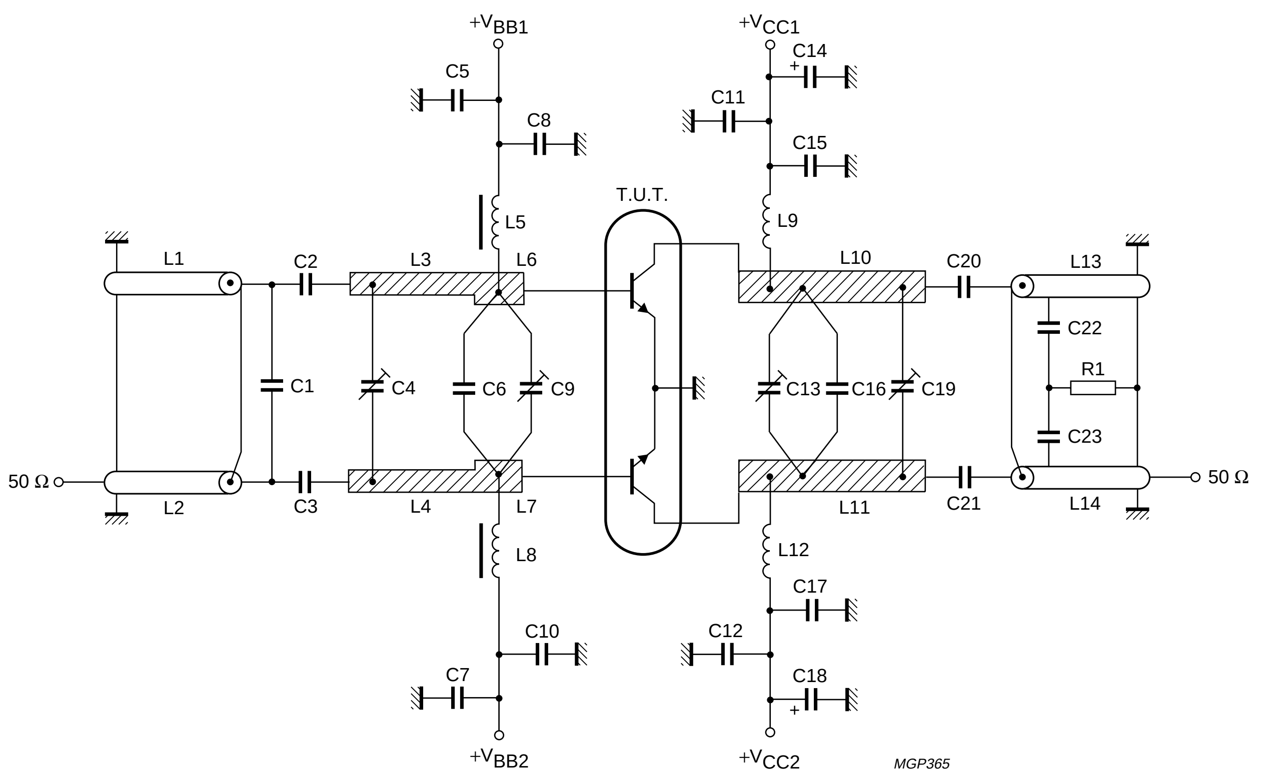


Fig.9 Class-A test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C6 = C16 = 4,7 pF (500 V) multilayer ceramic chip capacitor (ATC[1])

C2 = C3 = C20 = C21 = 33 pF multilayer ceramic chip capacitor (cat. no. 2222 851 13339)

C4 = C9 = C13 = C19 = 1,2 to 3,5 pF film dielectric trimmer (cat.no. 2222 809 05001)

C5 = C7 = C15 = C17 = 100 nF multilayer ceramic chip capacitor (cat. no. 2222 852 59104)

C8 = C10 = C11 = C12 = 220 pF multilayer ceramic chip capacitor (cat. no. 2222 852 13221)

C14 = C18 = 6,8 μF/40 V solid aluminium electrolytic capacitor

C22 = C23 = 1 pF (500 V) multilayer ceramic chip capacitor (ATC[1])

C9 and C13 are placed 8,0 and 14,0 mm from transistor edge, respectively.

L1 = L2 = L13 = L14 = 50 Ω semi-rigid cable; outer diameter 2,2 mm; length 29,0 mm. These cables are soldered on 75 Ω striplines (1,1 mm × 28,0 mm). The centre conductors of the cables L1 and L13 are not connected.

L3 = L4 = 52 Ω stripline (2,0 mm × 16,5 mm)

L5 = L8 = 470 nH microchoke

L6 = L7 = 39 Ω stripline (3,1 mm × 8,0 mm)

L9 = L12 = 1 turn Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 × 3,5 mm

L10 = L11 = 39 Ω stripline (3,1 mm × 34,0 mm)

L3, L4, L6, L7, L10 and L11 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,74); thickness 1/32".

R1 = 10 Ω carbon resistor

Note

1. ATC means American Technical Ceramics.

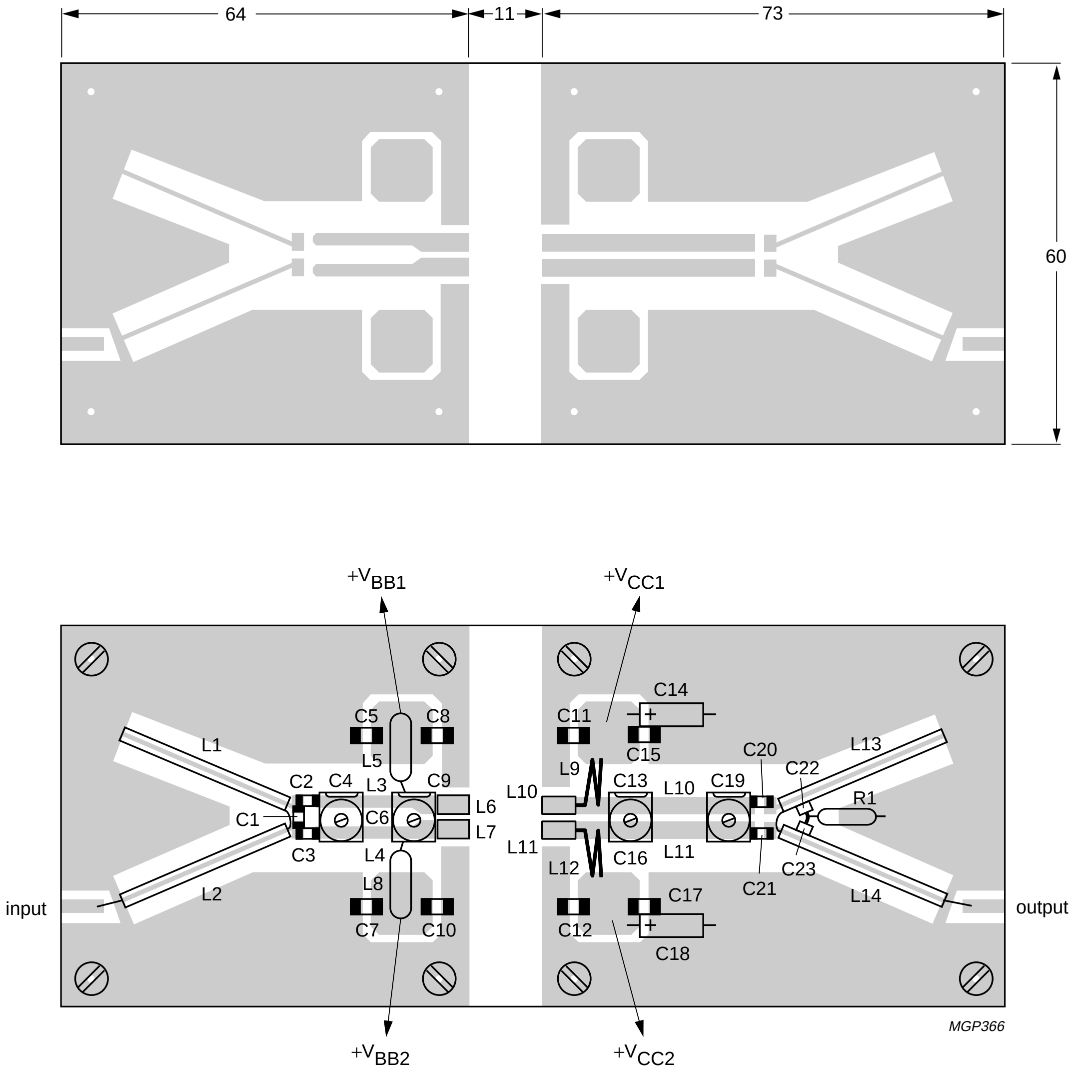


Fig.10 Component layout and printed-circuit board for 860 MHz class-A test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board, the other side is unetched copper to serve as a ground-plane. Earth connections are made by means of bolts. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

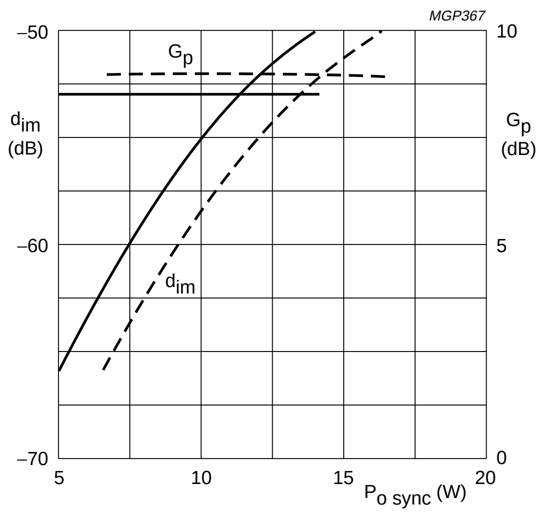


Fig.11 Intermodulation distortion (d_{im})[1] and power gain as a function of output power.

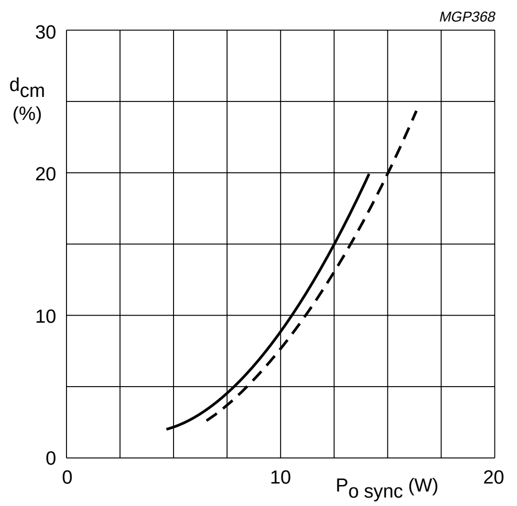


Fig.12 Cross-modulation distortion (d_{cm})[2] as a function of output power.

Conditions for Figs 11and 12:

Typical values; V_{CE} = 25 V; I_C = 2 × 0,85 A; – – – T_h = 25 °C; —— T_h = 70 °C; f_{vision} = 860 MHz.

Ruggedness in push-pull class-A operation

The BLV57 is capable of withstanding full load mismatch (VSWR = 50 through all phases) under the following conditions:

V_{CE} = 25 V; I_C = 2 × 0,85 A; T_h = 70 °C; $P_{o\ sync}$(1) ≤ 12,5 W; f = 860 MHz; $R_{th\ mb\text{-}h}$ = 0,25 K/W.

At any other composition of the output signal: P_L (r.m.s. value) ≤ 5 W.

Notes

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak sync level.
   Intermodulation distortion of input signal ≤ –70 dB.
2. Two-tone test method (vision carrier 0 dB, sound carrier –7 dB), zero dB corresponds to peak sync level.
   Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to –20 dB.

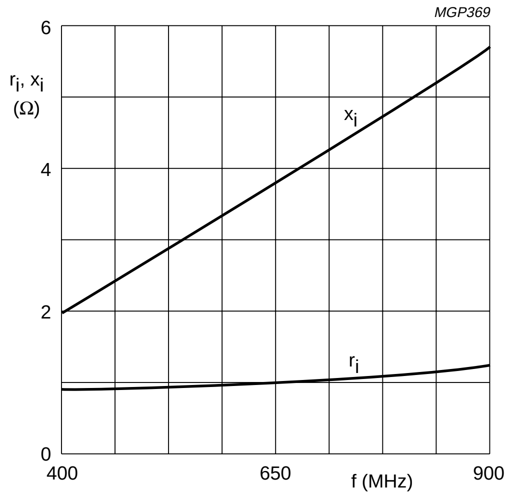


Fig.13 Input impedance (series components).

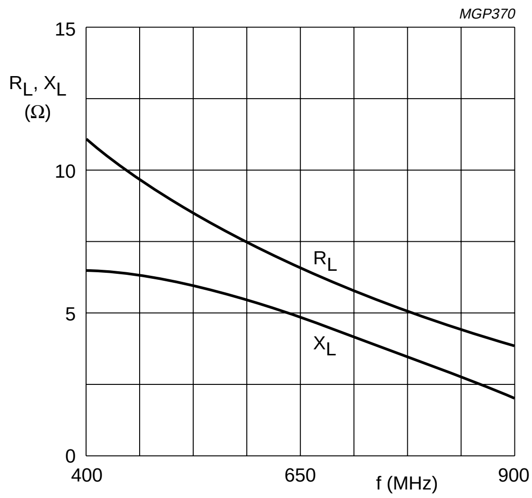


Fig.14 Load impedance (series components).

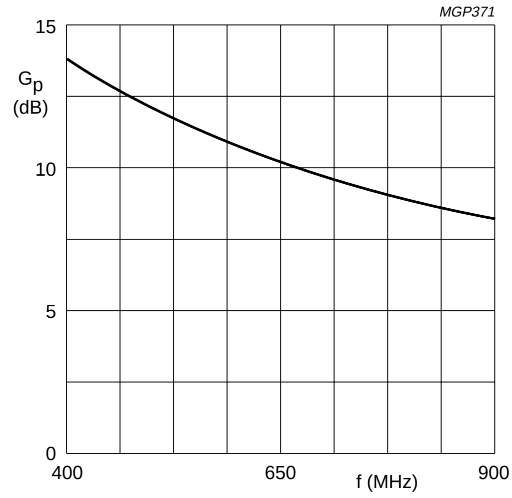


Fig.15

Conditions for Figs 13, 14 and 15:

The graphs apply to either transistor section assuming class-A push-pull operation.
Typical values; V_{CE} = 25 V; I_C = 0,85 A; T_h = 70 °C.

APPLICATION INFORMATION

R.F. performance in u.h.f. class-AB operation (c.w.)

f_{vision} (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (A)	T_h (°C)	P_L (W)	$I_{C1} = I_{C2}$ (A)	η (%)	G_p(1) (dB)
860	25	2 × 0,1	25	12,5			typ. 7,5
				38	typ. 1,25	typ. 60	typ. 6,5
860	25	2 × 0,1	70	12,5			typ. 7,0
				30	typ. 1,10	typ. 55	typ. 6,0

Note

1. Typical values are based on 1 dB gain compression. Using a 3rd order amplitude transfer characteristic, 1 dB compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, C.C.I.R. system).

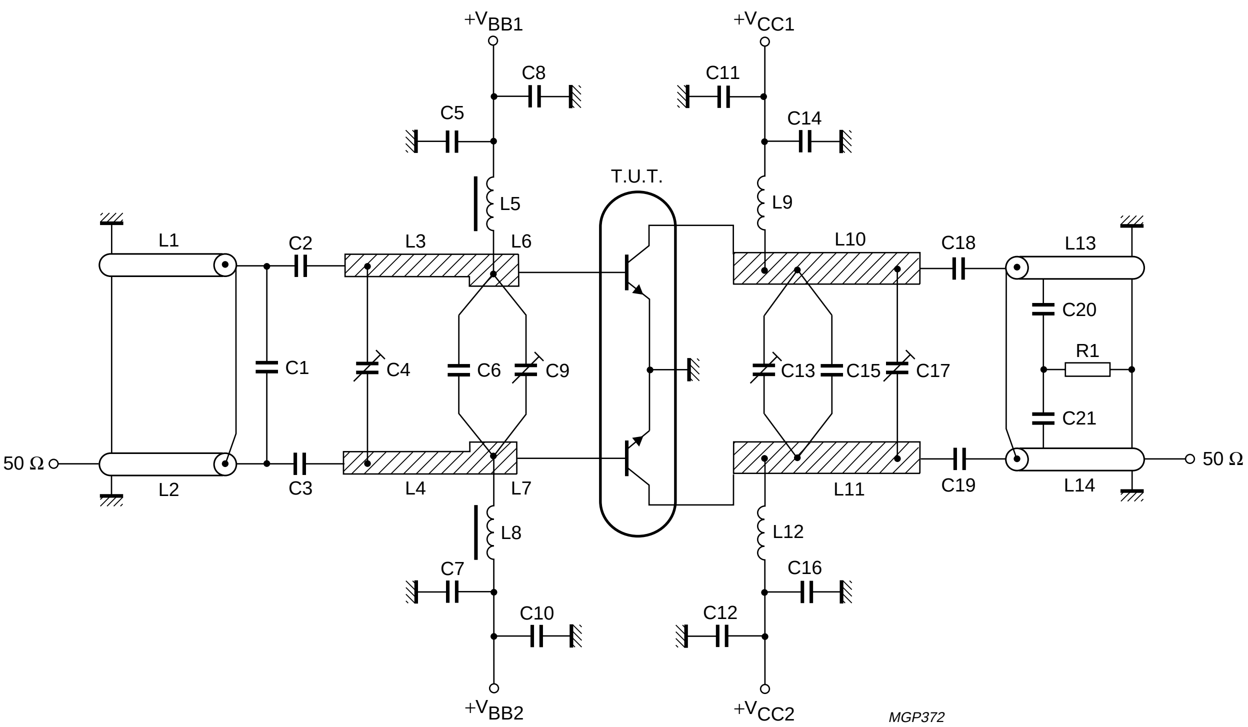


Fig.16 Class-AB test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C6 = C15 = 4,7 pF (500 V) multilayer ceramic chip capacitor (ATC[1])

C2 = C3 = C18 = C19 = 33 pF multilayer ceramic chip capacitor (cat. no. 2222 851 13339)

C4 = C9 = C13 = C17 = 1,2 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001)

C5 = C7 = C14 = C16 = 100 nF multilayer ceramic chip capacitor (cat. no. 2222 852 59104)

C8 = C10 = C11 = C12 = 220 pF multilayer ceramic chip capacitor (cat. no. 2222 852 13221)

C20 = C21 = 1 pF (500 V) multilayer ceramic chip capacitor (ATC[1])

C9 and C13 are placed 8,0 and 14,0 mm from transistor edge, respectively.

L1 = L2 = L13 = L14 = 50 Ω semi-rigid cable; outer diameter 2,2 mm; length 29,0 mm. These cables are soldered on 75 Ω striplines (1,1 mm × 28,0 mm). The centre conductors of the cables L1 and L13 are not connected.

L3 = L4 = 52 Ω stripline (2,0 mm × 16,5 mm)

L5 = L8 = 470 nH microchoke

L6 = L7 = 39 Ω stripline (3,1 mm × 8,0 mm)

L9 = L12 = 1 turn Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 × 3,5 mm

L10 = L11 = 39 Ω stripline (3,1 mm × 34,0 mm)

L3, L4, L6, L7, L10 and L11 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,74); thickness 1/32”

R1 = 10 Ω carbon resistor.

Note

1. ATC means American Technical Ceramics.

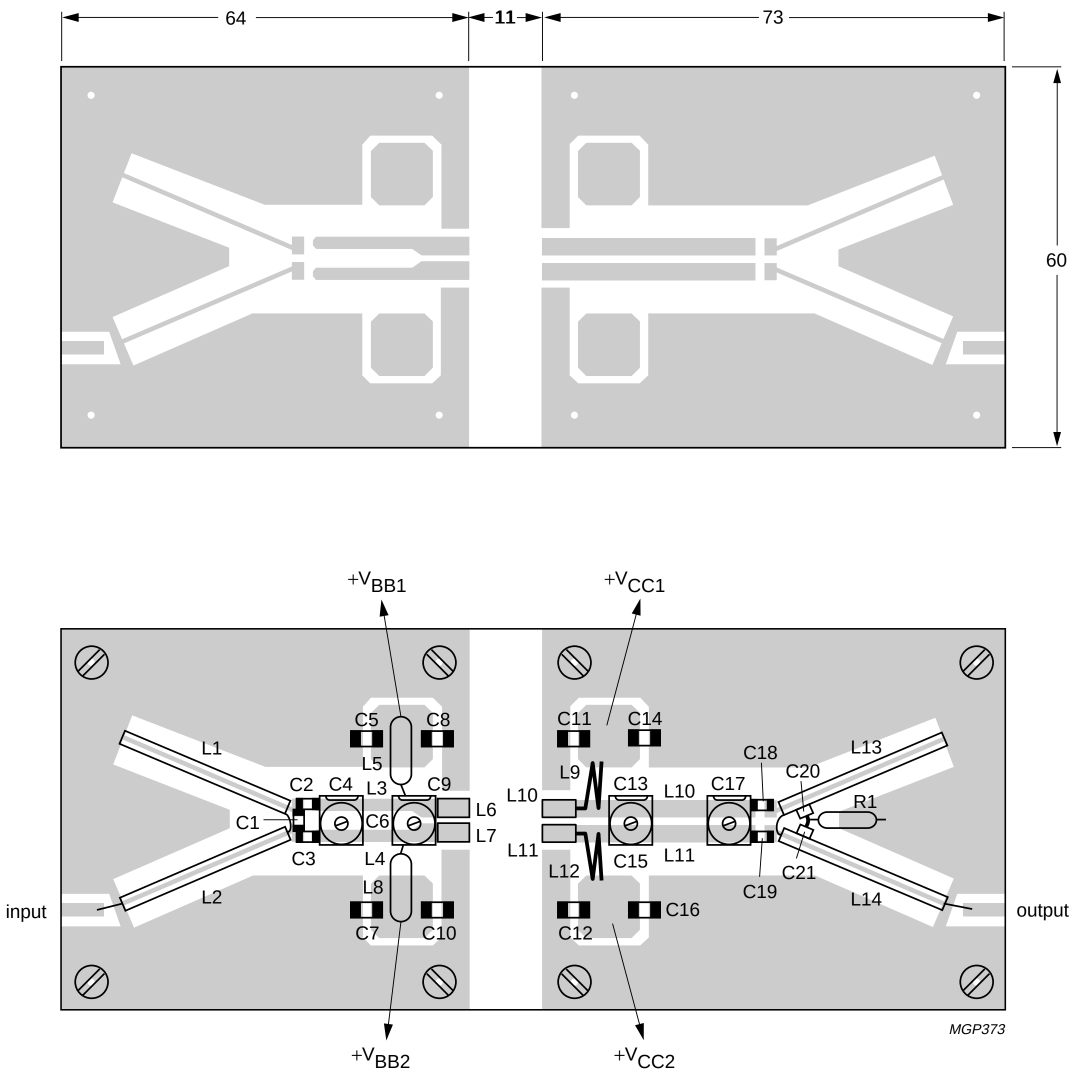


Fig.17 Component layout and printed-circuit board for 860 MHz class-AB test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board, the other side is unetched copper to serve as a ground-plane. Earth connections are made by means of bolts. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

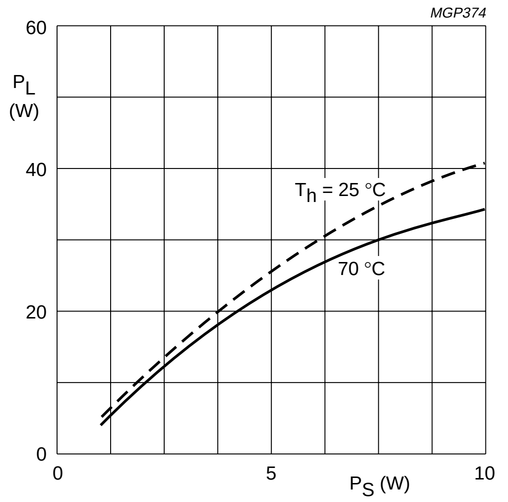


Fig.18 Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 2 × 0,1 A; f_{vision} = 860 MHz.

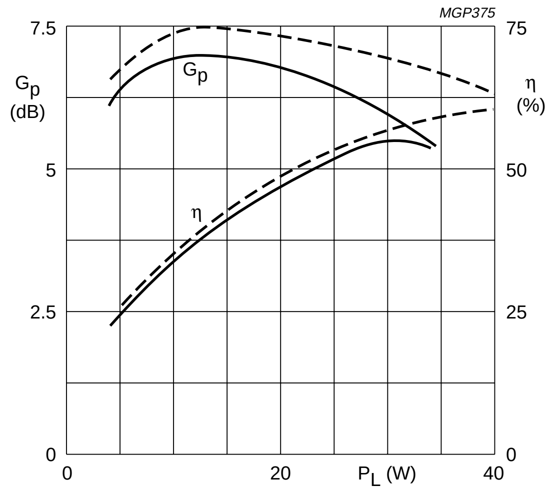


Fig.19 Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 2 × 0,1 A; – – – T_h = 25 °C; ——— T_h = 70°C; f_{vision} = 860 MHz.

Ruggedness in class-AB operation

The BLV57 is capable of withstanding a load mismatch (VSWR ≤ 2 through all phases) up to 30 W (r.m.s. value) or (VSWR ≤ 50 through all phases) up to 19 W under the following conditions:
V_{CE} = 25 V; T_h = 70 °C; f = 860 MHz; $R_{th\ mb\text{-}h}$ = 0,25 K/W.

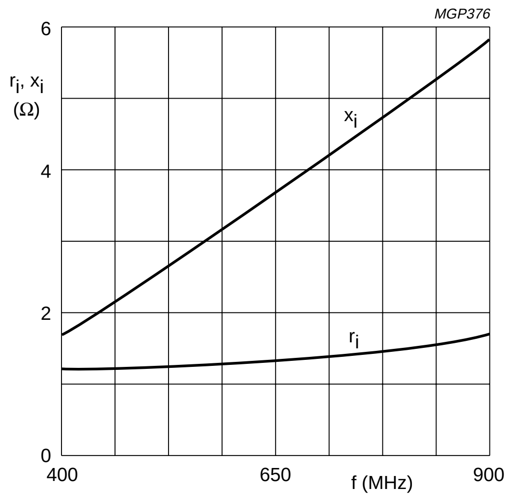


Fig.20 Input impedance (series components).

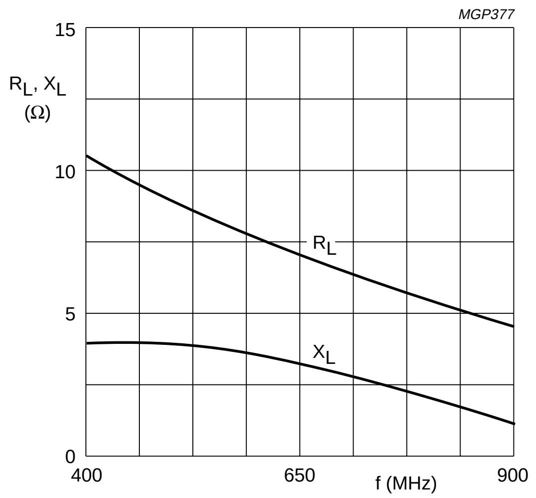


Fig.21 Load impedance (series components).

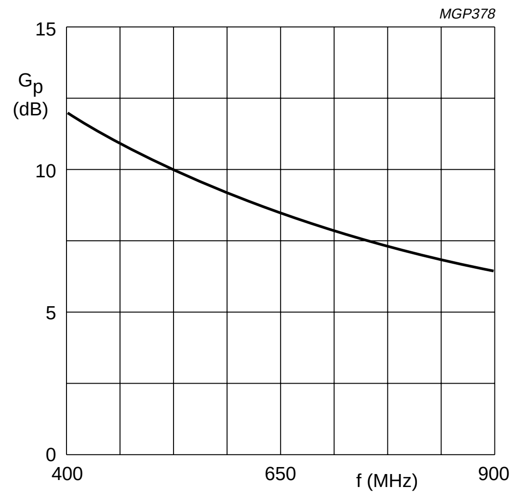


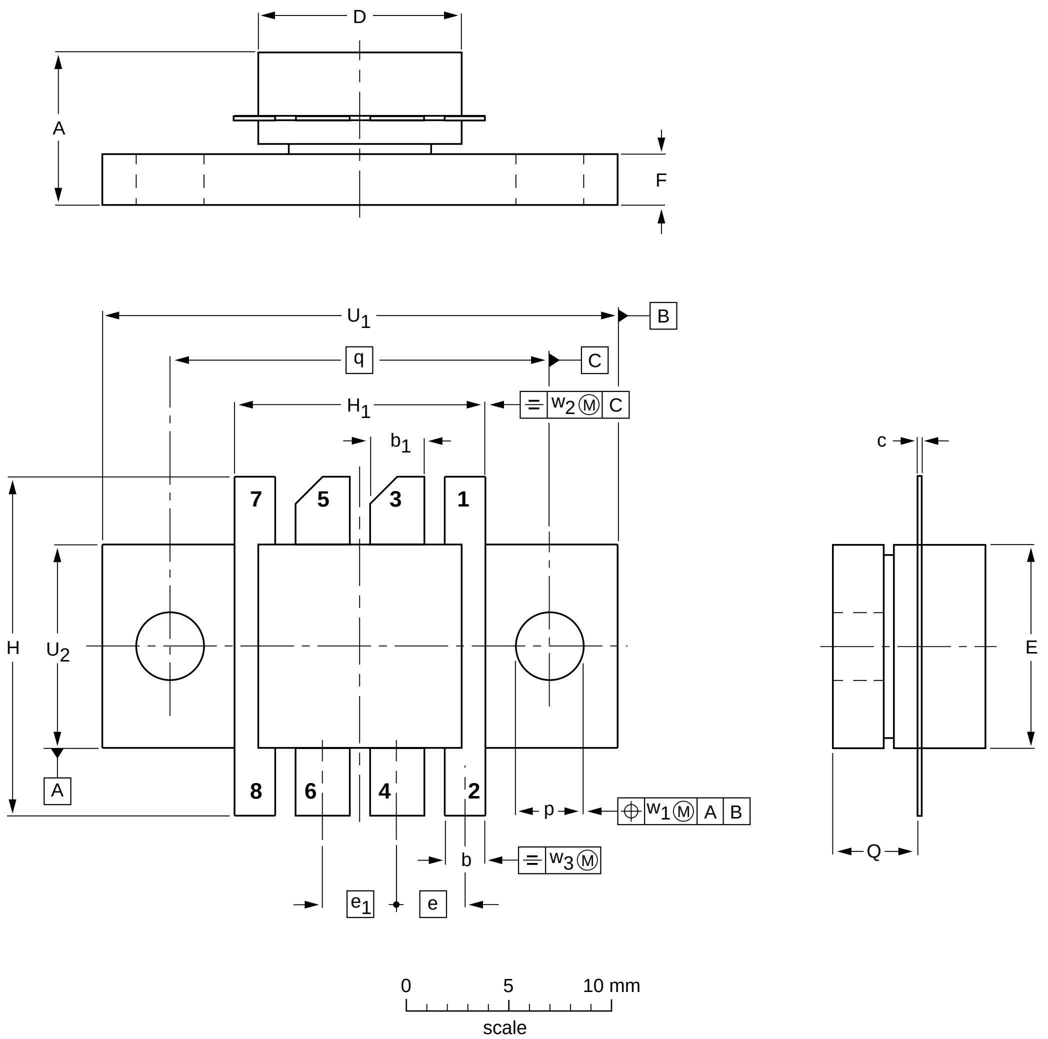
Fig.22

Conditions for Figs 20; 21 and 22:

The graphs apply to either transistor section assuming class-AB push-pull operation.
Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 0,1 A; P_L = 17,5 W (P.E.P); T_h = 70 °C.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 8 leads **SOT161A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	E	e	e_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	7.27 6.47	2.04 1.77	2.93 2.66	0.18 0.10	10.22 10.00	10.22 10.00	3.50	3.80	2.70 2.08	17.00 16.00	12.83 12.57	3.36 2.92	4.32 4.06	18.42	24.97 24.71	10.34 10.08	0.51	1.02	0.26
inches	0.286 0.255	0.080 0.070	0.115 0.105	0.007 0.004	0.402 0.394	0.402 0.394	0.138	0.150	0.106 0.082	0.669 0.630	0.505 0.495	0.132 0.120	0.170 0.160	0.725	0.983 0.973	0.407 0.397	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT161A						97-06-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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